

Abstracts

Evaluation of Excess Inductance and Capacitance of Microstrip Junctions (Short Papers)

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Excess inductance and capacitance of various microstrip discontinuities (bends, impedance steps, and simple vias) are evaluated. For the inductance calculations, the structure is assumed to consist of perfectly conducting foils located in vacuum above a perfectly conducting ground plane. For the capacitance calculations, the structure is assumed to be embedded in a multilayered dielectric medium. The surface-current distribution for the excess inductance calculation and the surface-charge distribution for the capacitance calculation are evaluated numerically, solving integral equations based on the boundary conditions. Thereby, the conductor and dielectric surfaces are divided into a number of triangles, and the point-matching technique is used.

[Return to main document.](#)